CLAIMS

What is claimed is:

1. A system for loading firmware in a high availability system comprising:

a high speed interconnect;

a mismatched cell coupled to the high speed interconnect and comprising errored firmware, the mismatched cell configured to enable the high speed interconnect;

an update cell coupled to the high speed interconnect and comprising update firmware, the update cell configured to load the update firmware to the mismatched cell via the high speed interconnect at a first rendezvous; and

a boot block configured to reset the mismatched cell and the update cell through to the first rendezvous.

2. The system of claim 1 wherein the system further comprises correction firmware configured to determine that processor dependent code is not resident on the high availability system and, in response, to boot the boot block.

3. The system of claim 1 wherein the system further comprises processor dependent code and correction firmware, the correction firmware configured to determine that a checksum for the processor dependent code is not correct and, in response, to boot the boot block.

4. The system of claim 1 wherein the update cell further is configured to determine at the first rendezvous that the update firmware is a desired version of firmware and, thereafter, to load the update firmware to the mismatched cell via the high speed interconnect.

5. The system of claim 1 further comprising a second mismatched cell comprising second errored firmware, the second mismatched cell configured to enable the high speed interconnect;

wherein the boot block further is configured to reset the second mismatched cell only through to the first rendezvous; and

wherein the update cell further is configured to load the update firmware to the second mismatched cell via the high speed interconnect.

6. The system of claim 1 wherein the errored firmware comprises at least one member of a group consisting of firmware that is not a latest version of firmware and corrupt firmware.

7. The system of claim 1 further comprising:

a manageability system interconnect;

wherein the mismatched cell is configured to receive an update message via the manageability system interconnect and, in response thereto, to transmit an acknowledgement via the manageability system interconnect and to enable the high speed interconnect; and

wherein the update cell further is configured to generate an update menu, to receive an update command generated via the update menu, and, in response thereto, to transmit the update message to the mismatched cell and, after receiving the acknowledgment, to load the update firmware to the mismatched cell via the high speed interconnect.

8. The system of claim 1 further comprising:

a manageability system interconnect;

wherein the mismatched cell further is configured to receive an update message via the manageability system interconnect and, in response thereto, to enable the high speed interconnect; and

wherein the update cell further is configured to transmit the update message to the mismatched cell and, thereafter, to automatically load the update firmware to the mismatched cell via the high speed interconnect.

9. A method for loading firmware in a high availability system comprising a high speed interconnect and at least a mismatched cell and an update cell, the mismatched cell coupled to the high speed interconnect and comprising errored firmware such that the high speed interconnect is not enabled for the mismatched cell, the update cell coupled to the high speed interconnect and comprising update firmware, the method comprising:

using a boot block to reset the mismatched cell and the update cell to a first rendezvous;

enabling the high speed interconnect from the mismatched cell at the first rendezvous; and

loading the update firmware from the update cell to the mismatched cell via the high speed interconnect.

10. The method of claim 9 further comprising using correction firmware to determine that processor dependent code is not resident on the high availability system and, thereafter, resetting the mismatched cell and the update cell to the first rendezvous using the boot block.

11. The method of claim 9 further comprising determining that a checksum for processor dependent code is not correct and, thereafter, resetting the mismatched cell and the update cell to the first rendezvous using the boot block.

12. The method of claim 9 further comprising determining at the first rendezvous that the update firmware is a desired version of firmware and, thereafter, loading the update firmware to the mismatched cell via the high speed interconnect.

13. The method of claim 9 further comprising:

enabling the high speed interconnect by a second mismatched cell comprising second errored firmware; and

loading the update firmware from the update cell to the second mismatched cell via the high speed interconnect to replace the second errored firmware.

14. The method of claim 9 further comprising replacing with the update firmware at least one member of a group consisting of firmware that is not a latest version of firmware and corrupt firmware.

15. The method of claim 9 further comprising:

generating an update menu;

receiving an update command generated via the update menu and, in response thereto, transmitting an update message to the mismatched cell via a manageability system interconnect;

receiving the update message at the mismatched cell and, in response thereto, transmitting an acknowledgement via the manageability system interconnect and enabling the high speed interconnect;

receiving the acknowledgment at the update cell; and

loading the update firmware from the update cell to the mismatched cell via the high speed interconnect.

16. The method of claim 9 further comprising:

transmitting an update message to the mismatched cell via a manageability system interconnect;

receiving the update message at the mismatched cell and, in response thereto, enabling the high speed interconnect; and

automatically loading the update firmware from the update cell to the mismatched cell via the high speed interconnect.

17. A method for loading firmware in a high availability system comprising a manageability system, a high speed interconnect, and a plurality of cells, the plurality of cells each coupled to the manageability system and coupled to the high speed interconnect but not enabled for the high speed interconnect, the method comprising:

loading a boot block via the manageability system to at least a first memory location of at least a first cell;

loading update firmware via the manageability system to at least a second memory location of at least an update cell;

using the boot block of the first cell to reset the cells to a first rendezvous;

enabling the high speed interconnect for the cells at the first rendezvous; and

loading the update firmware from the update cell to the other cells via the high speed interconnect.

18. The method of claim 17 further comprising loading the boot block to other first memory locations of a plurality of the cells via the manageability system.

19. The method of claim 17 further comprising:

loading the boot block to other first memory locations of only other cells that do not have a desired version of firmware; and

loading the update firmware to other second memory locations of only other cells that do not have the desired version of firmware.

20. The method of claim 17 wherein the loading the boot block to the first memory location comprises at least one member of a group comprising loading the boot

block to a non-volatile memory location and loading the boot block to a firmware storage element location.

21. The method of claim 17 wherein the loading the update firmware to the second memory location comprises at least one member of a group comprising loading the update firmware to a non-volatile memory location and loading the update firmware to a firmware storage element location.

22. The method of claim 17wherein first cell is the update cell and the step of loading the update firmware via the manageability system to the second memory location of the update cell comprises loading the update firmware via the manageability system to the second memory location of the first cell.